A Si BJT IF DOWNCONVERTER/AGC IC FOR DAB

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ABSTRACT

A low cost, 920 MHz to 30 MHz downconverter/AGC IF IC of novel topology is described. Implemented in Si bipolar technology, this device provides 85 dB of conversion gain, a 15 dB NF (including the 22dB loss of an external bandpass filter), a leveled output of 41 dBmV (120 mVrms), with a minimum IM ratio of 40 dB. With a companion RFIC , it forms a DAB receiver.

INTRODUCTION

This paper describes an IF circuit which, when combined with a dual band RF front end chip [1], accurately receives Digital Audio Broadcasting (DAB) signals from -97 dBm with an output S/N ratio of 8 dB, to -10 dBm with an output intermodulation (IM) ratio [2] exceeding 40 dB**.** This novel receiver architecture [3] eliminates expensive tunable preselect filters which would increase receiver cost and size. Assembled into plastic, 28 pin SSOP packages, these devices [4] provide a low cost solution for manufacturers seeking to add L-band (~1470 MHz) and Band III (~200 MHz) DAB functionality to a "dashboard compatible" mobile receiver solution.

Implemented using a low cost, 25 GHz f_t Silicon bipolar process [5], this circuit provides conversion of the 920 MHz first IF input signal to a 30 MHz second IF output signal, with up to 63 dB of net small signal conversion gain which includes the 22 dB loss of the 30 MHz, 1.5 MHz wide, SAW based channel bandpass filter (BPF). The measured noise figure (NF) is less than 15 dB under high gain conditions. AGC action is carefully designed to achieve minimum degradation of NF over the full 54 dB range of gain control to a leveled output of 41dBmV (120mVrms) into a high capacitance load (e.g. A/D converter), with a minimum IM ratio of 40 dB. The circuit, together with two external capacitors, contains all the circuitry to autonomously provide the AGC functions. External signals are: a 24 MHz system reference clock, the AGC_pause and Power_management digital control inputs and DC power supplies.

While there is considerable prior art on the use of AGC circuits in IF sections, the increased complexity of implementing multiple AGC stages at UHF frequencies in an integrated form has discouraged the use of this architecture.

CHIP TOPOLOGY

The block diagram of the chip (Figure 1) shows the major functions of the IF IC: The signal path is comprised of the **LNA/Mixer**, the **1st AGC**, and the **2nd AGC** stages. The **Synthesizer** consists of a bipolar VCO and a PLL to provide a fixed, low phase noise local oscillator (LO) for the downconversion mixer which is phase locked to the system reference clock. The **Control circuits** provide the output level range as well as the power management and AGC pause control functions which conserve DC power and retain AGC level information, respectively, insuring rapid re-acquisition during short term signal losses. Additionally, there is a bandgap referenced, 3.3V voltage regulator circuit to supply DC power to both the internal LO and other external (e.g. RFIC) system components. The specifics of these functional blocks are discussed in the following sections.

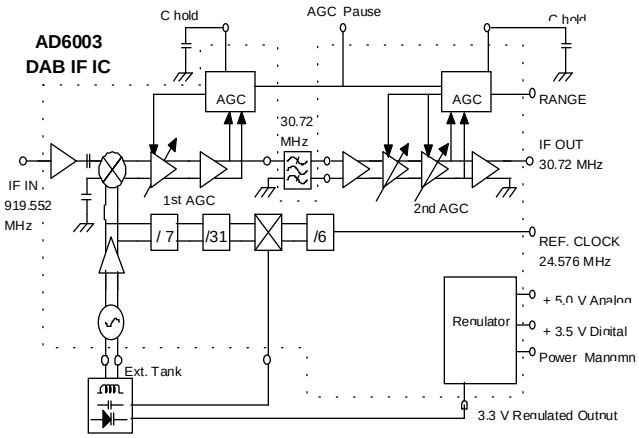

Figure 1 - IF Downconverter/AGC Chip Block Diagram.

LNA/MIXER DESIGN

A simplified schematic of the LNA/Mixer stage is shown in Figure 2. The LNA consists of a cascode connection of two NPN transistors buffered by an emitter follower. Feedback is employed by coupling the output of the emitter follower to the input of the cascode through an R-C network. This single ended configuration provides approximately 8 dB of voltage gain while maintaining a match at the input of the LNA.

One input to the mixer is AC coupled to the single ended output of the LNA, while the other is AC grounded. The mixer is a conventional Gilbert cell design employing emitter degeneration and a buffered LO input circuit to

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reduce loading the VCO and to provide adequate voltage swing to the mixer. The output is fed to the 1st AGC stage as a balanced signal. In this configuration, the voltage gain of the mixer is reduced by 6 dB by this single ended to balanced conversion, retaining approximately 2 dB of voltage gain in the mixer.

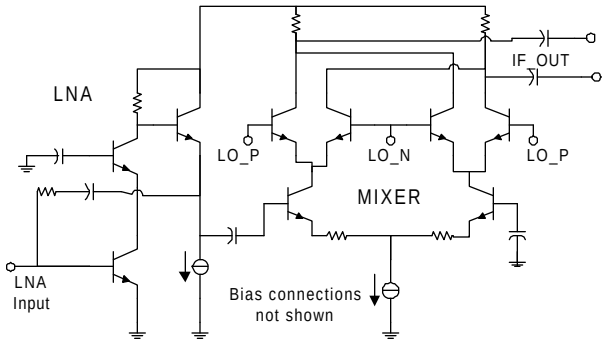

Figure 2 - Simplified Schematic of the LNA / Mixer Stage.

1ST AGC AMPLIFIER DESIGN

The 1st AGC amplifier consists of a single stage, emitter degenerated differential amplifier. The balanced output of this amplifier drives the SAW filter, and is also low pass filtered and applied to a detector circuit which adjusts the gain to maintain a leveled output of approximately 70 mVrms (37 dBmV) over a 13 dB control range. The gain control is implemented by varying the transconductance of the 10:1 triplet which forms the active section of the AGC amplifier shown as a differential pair in Figure 3.

The output is leveled to a value represented by V_{ref} by charging or discharging an external capacitor C_{hold}. A low level input signal causes C_{hold} to charge up to its maximum level which results in a voltage gain for the stage of 18 dB. Under the application of a high level signal, the storage capacitor is discharged and the gain drops to a minimum of 5 dB. By carefully selecting the capacitor value, system time constants can be selected to optimize performance.

The combination of LNA/Mixer/1st AGC amplifier produces an 13 dB variable voltage gain stage from +5 to +18 dB with an associated NF of 11 dB at the high gain setting. The IM ratio of this section of the circuitry exceeds 50 dB up to input levels of -15 dBm. The 300 Ω, single ended output of this stage is applied to the 30 MHz BPF for adjacent channel rejection of nearby interferers.

2ND AGC AMPLIFIER DESIGN

The balanced output of the 30 MHz BPF is applied to the input of the 2nd AGC amplifier. This circuit is similar to the 1st AGC amplifier design with the addition of a second variable gain section and some additional fixed gain in the input and output buffer stages. Overall, this amplifier has a voltage gain of approximately 66 dB with 36 dB of gain control, more than twice the control range of the 1st AGC amplifier.

A range control pin is provided which adjusts the output level of this circuit. This capability provides the RF system engineer the opportunity to optimize the output level of the IC to match the dynamic range of the A/D converter following the IC. When the pin is floating, the output is leveled to approximately 120 mVrms across a 1K ‖ 25 pF load. By connecting the range pin to ground or +5V through a suitable resistance, the leveled output voltage can be adjusted over a +/-10 dB range from 40 mVrms to 400 mVrms.

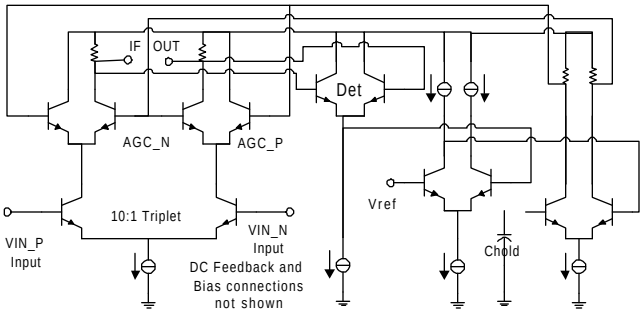

Figure 3- Simplified Schematic of an AGC/Detector Stage.

SYNTHESIZER DESIGN

The synthesizer is used to supply the 888 MHz LO signal used by the mixer. The 888.8 MHz VCO and 24.6 MHz reference clock signals are divided by 217 and 6, respectively, resulting in a 4.1 MHz compare frequency.

The VCO, which is similar to an earlier design [6], employs a pair of cross coupled collector, differentially connected, bipolar transistors to realize a balanced Colpitts oscillator, coupled to an external tank circuit. The external tank consists of a parallel tuned LC resonator whose inductance can be realized in the form of a lumped “chip” inductor or a printed microstrip line. The tuning capacitance is provided by a high-Q, abrupt junction varactor diode, minimizing phase noise. Greater than 70 MHz of tuning range is obtained. This is more than adequate to account for component yield and temperature performance variations associated with low cost, off chip components. Even with this wide tuning range, phase noise performance of better than -100 dBc/Hz at 100 KHz offset is realized. The VCO is biased from an internal 3.3 V regulator which is capable of sourcing up to 30 mA, and can provide a “clean” supply to power external circuits such as the VCO in the RF chip. The divider circuits are realized using a combination of balanced emitter coupled logic gates operating over small AC voltage swings to achieve divider operation at 888 MHz. The VCO divider is a divide by 217 circuit implemented as a cascade of a fast divide by 7 and a divide

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by 31. The divide by 31 circuit incorporates a variable modulus divide by 5 or divide by 8 topology with the appropriate feedback to realize the combined function. The 3.5V compatible CMOS reference clock input at 24 MHz is applied to a divide by 6 employing similar divider circuits.

The 4.096 MHz outputs of the two dividers are applied to a phase/frequency detector consisting of a pair of flip flops with the appropriate reset inputs. The two phase detector up and down outputs are applied to a charge pump which steers a current of up to 250 µA to the off-chip loop filter. This filter converts the current to a voltage which controls the varactor diodes in the VCO.

CONTROL CIRCUITS

Separate bandgap references are provided on-chip and are appropriately buffered to avoid loading or coupling between undesired parts of the circuit. Circuits which are associated with the divider circuitry are isolated by separate power and ground lines from those parts of the circuit which are responsible for low noise operation. Great care was taken for the 1st and 2nd stage AGC amplifier power and ground connections, as well as the LNA/Mixer connections, to avoid coupling high level IF output signal levels back into earlier stages.

Under normal operation, the IFIC requires two DC supplies: an analog supply of 5V at 75 mA to power all the signal path circuits and the regulator which supplies the VCO; and a digital supply of 3.5 V @ 25 mA to power the dividers and PLL circuitry. Power management is implemented which shuts down the LNA/Mixer chain during periods of inactivity to reduce DC current consumption from the 5V supply by 40 mA.

An AGC_pause function is provided which operates similar to a sample and hold circuit. During normal operation, the gain of the AGC circuits is established by injecting or removing charge from a hold capacitor. This capacitor is external to the IC to allow the user to individually determine system time constants. Under AGC_pause operation, the AGC loop is disabled and the gain is frozen at the current value. The leakage current in this mode is less than 10 nA. This allows the circuit to be used in applications where the received signal may not be present at all times, such as paging or digital messaging over a DAB channel. Additional functions related to signal acquisition and dual band operation are implemented and discussed in reference [4].

CHIP PERFORMANCE

Measurements on several thousand parts show that the small signal gain for the chain is 62.4 +/- 0.7 dB with an associated noise figure of 14.5 dB. Small signal gain and noise figure vary by less than -0.04 dB/°C, and +0.04 dB/°C, respectively, over a range of -55 to +100 °C. The IM ratio is greater than 40 dB up to an input power level of -17 dBm. DC power dissipation is 400 mW typical under normal operation and drops to 200 mW typical in the power management mode.

Figure 4 shows typical voltage gain, output voltage, and IM performance for the IF chip, including the 30 MHz BPF with a 22dB loss. As the input power increases, the gain is constant until the gain control threshold is reached at approximately -68 dBm. At this point, the gain of the second IF stage begins to drop at 1 dB per dB of input power and the output voltage and IM ratio flatten out. This behavior is analogous to placing an attenuator immediately preceding the last output stage.

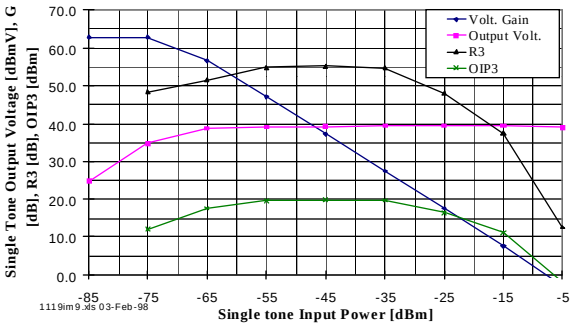

Figure 4 - Output Voltage, Voltage Gain, IM Ratio and Output Intercept Point vs. Input Power for the IF Chip.

The gain of the second AGC stage continues to fall until the threshold of the first AGC amplifier is reached at about -45 dBm input. At this point, the gain, NF, and IM ratio of the second amplifier become constant and the 1st AGC amplifier takes over for the remainder of the gain control region. The careful design of the overlap region insures that the second stage does not over-attenuate which would limit the IM performance. It also insures that the first stage does not attenuate at too low an input power, which would limit the noise figure. Figure 5 shows the change in noise figure as a function of gain reduction. This demonstrates that the overall NF degrades considerably less than one dB/dB of gain reduction insuring an improving C/N ratio for the system as the input power increases. This careful control of the system gain coupled with a similar circuit in the RF chip, which was designed in concert with it, results in optimization of both system noise and IM performance even in the presence of significant adjacent channel

interferers.

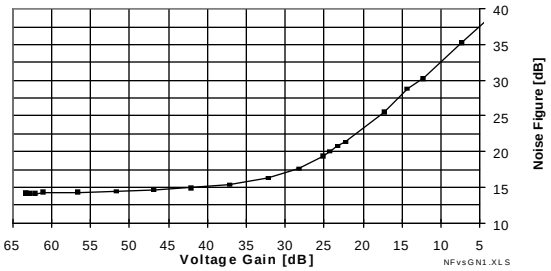

Figure 5 - IF IC Noise Figure vs. Voltage Gain.

DEVICE TECHNOLOGY

The IFIC is fabricated using Analog Devices "ADRF", a 25 GHz f_t, Silicon Bipolar Process [5]. This is a junction isolated, double metal, 0.5 μm emitter process implemented on 6" wafers. In addition to NPN devices, this process provides high and low sheet resistivity poly-Si resistors, lateral PNP devices, and MOS capacitors.

Device packaging utilizes a plastic SSOP-28 package molded over a standard copper lead frame, which is later solder plated. Assembly utilizing high volume, digital circuit techniques contributes to low manufacturing costs. Testing is accomplished using automated handlers, a specially designed high frequency test socket, and a PC board capable of operation to over 900 MHz. Extensive RF and DC characterization using automated RF testing requires less than 4 seconds per part.

CONCLUSIONS

An IF IC has been presented which provides down conversion from 920 MHz to 30 MHz and autonomous AGC functions which have been carefully designed to optimize noise figure and IM performance over a wide dynamic range. The circuit is fabricated using a standard Si bipolar process, then packaged and tested using industry standard techniques to minimize component cost. This circuit, together with an RFIC, implements a novel DAB tuner architecture which eliminates preselection filtering, thus reducing system costs. These parts enable the low cost manufacture of a DAB receiver front end, which provides the addition of L-band and Band III capability to a standard receiver. When combined with a digital processing ASIC, the resulting module fits into the standard, 50mm high DIN outline of an automobile radio.

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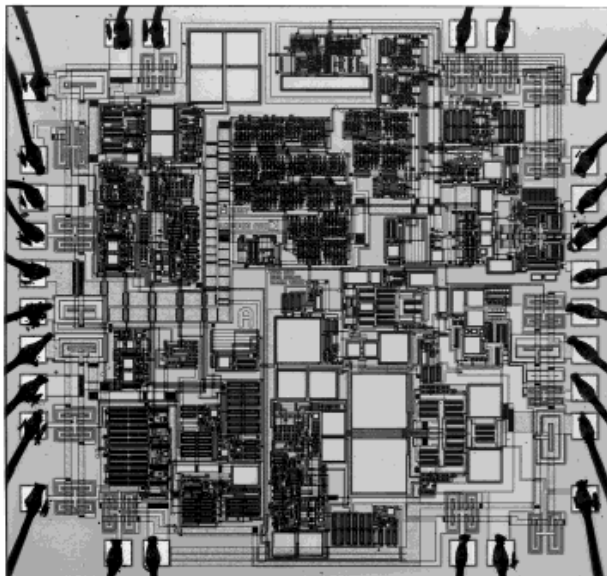

Figure 6 - Die Photo of Downconverter/AGC IF Chip.

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